OK TO ENTER: /JK/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Derick G. Behrends et al.
Serial No.	:	10/636,060
Filed	:	August 7, 2003
For	:	METHODS AND APPARATUS FOR TESTING INTEGRATED CIRCUITS
Examiner	:	James C. Kerveros
Group Art Unit	:	2117
Customer No.	:	46628

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. 1.312

Sir:

In response to the Notice of Allowance and Issue Fee Due mailed on April 21, 2008, Applicants submit this Rule 312 Amendment.

Amendments to the Claims begin on page 2
Remarks begin on page 6

A M E N D M E N T

IN THE CLAIMS:

Please cancel claims 13-21 without prejudice so that the claims read as follows:

1. (Previously presented) A method for testing an integrated circuit (IC) comprising:

selecting a bit during an ABIST test from each of a plurality of memory arrays formed on an IC chip;

selecting one of the plurality of memory arrays on the IC chip; and

storing the selected bit from the selected memory array_in a component of the IC chip wherein an outcome of the ABIST test is determined based on the stored selected bit.

2. (Original) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays includes selecting a wordline in each of the plurality of memory arrays.

3. (Original) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays includes overwriting an initial state bit value of a selection circuit with a value of the selected bit.

4. (Original) The method of claim 1 wherein storing the selected bit from the selected memory array includes storing the selected bit from the selected memory array in a latch.

5. (Original) The method of claim 4 wherein storing the selected bit from the selected memory array includes one of storing an initial state bit value of an output of a selection circuit and storing a modified initial state bit value of the output of the selection circuit in the latch.

6. (Previously presented) The method of claim 1 wherein selecting a bit from each of a plurality of memory arrays formed on an integrated circuit chip, selecting one of the plurality of memory arrays, and storing the selected bit from the selected memory array are performed during an ABIST test of the integrated circuit chip.

7. (Previously presented) A method for testing an integrated circuit (IC) comprising:

selecting a bit during an ABIST test from each of a first and second plurality of memory arrays formed on an IC chip;

selecting one memory array from each of the first and second plurality of memory arrays of the IC chip; and

storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays in a component of the IC chip wherein an outcome of the ABIST test is determined based on the stored selected bit.

8. (Original) The method of claim 7 wherein selecting a bit from each of the first and second plurality of memory arrays

includes selecting a wordline in each of the first and second plurality of memory arrays.

9. (Original) The method of claim 7 wherein selecting a bit from each of the first and second plurality of memory arrays includes:

overwriting a first initial state bit value with a value of the selected bit from the selected memory array of the first plurality of memory arrays; and

overwriting a second initial state bit value with a value of the selected bit from the selected memory array of the second plurality of memory arrays.

10. (Original) The method of claim 7 wherein storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays includes:

storing the selected bit from the selected memory array of the first plurality of memory arrays in a first latch; and

storing the selected bit from the selected memory array of the second plurality of memory arrays in a second latch.

11. (Original) The method of claim 10 wherein storing the selected bit from the selected memory array of the first plurality of memory arrays includes one of storing an initial state bit value of an output of a first selection circuit and storing a modified initial state value of the output of the first selection circuit in a first latch; and

wherein storing the selected bit from the selected memory array of the second plurality of memory arrays includes one of storing an initial state bit value of an output of a second selection circuit and storing a modified initial state value of the output of the second selection circuit in a second latch.

12. (Previously presented) The method of claim 7 wherein selecting a bit from each of a first and second plurality of memory arrays formed on an IC chip, selecting one memory array from each of the first and second plurality of memory arrays, and storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays are performed during an ABIST test of the IC chip.

13. to 21. (Canceled)

REMARKS

The April 21, 2008 Notice of Allowance allowed the following claims: 1-21. Claims 13-21 have been canceled herein without prejudice. No additional claims have been added, and no new matter has been added.

Applicants respectfully request entry of this amendment into the official record of the present application.

Applicants do not believe any fees are due regarding this amendment. If any fees are required, however, please charge Deposit Account No. 04-1696. Applicants encourage the Examiner to telephone Applicants' attorney to discuss the amendment should any issues remain.

Respectfully Submitted,

Steven M. Santisi
Registration No. 40,157
Dugan & Dugan, PC
Attorneys for Applicants
(914) 579-2200

Dated: May 28, 2008
Hawthorne, New York